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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,103	LAMBINO ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Power of Attorney dated 4/15/2003 and Change in Power of Attorney 3/10/2003.

2. Claims 1-28 are presented for examination.

Claim Objections

3. Claim 20 and 23 are objected to because of the following informalities:

a. As to claim 20, on line 6 it appears that following "boot" the word "block" should be inserted for clarity.

b. As to claim 23, on line 1, "20" should be changed to "22" for the claim to have proper antecedent basis. Currently claim 23 lacks proper antecedent basis because "backup battery" on line 2 of the claim lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 17-21 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller, U.S. Patent 6,308,265.

6. As to claim 20, Miller teaches a system comprising:

a. a processor (CPU) [col. 4 lines 45-49];

b. a flash memory comprising a primary location (first writable segment/first region) and a secondary location (second writable segment/second region) [col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3]; and

c. a boot block executed from the primary location wherein the boot block further:

i. is copied to the secondary location [col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3];

ii. points an execution address to the secondary location (CPU will boot from the secondary location, therefore an execution address must point to the secondary location) [col. 6 lines 4-10]; and

iii. copies a new boot block (update first block) to the primary location [figure 3 and col. 5 line 65 et seq.]

iv. points the execution address to the primary location (the PC will be allowed to boot from code in the primary location, therefore the execution address must point to the primary location) [col. 7 lines 4-7].

7. As to claim 21, Miller teaches the system according to claim 20, as described above. Miller further teaches an address conversion mechanism (boot in progress flag) for moving the execution address (flag determines where execution will begin) [col. 6 lines 2-10 and col. 7 lines 4-7].

8. As to claims 17 and 24, Miller taught the claimed system. Therefore, Miller also teaches the claimed method of using and the claimed article comprising a medium for storing instructions to enable such a system.

9. As to claim 18, Miller taught the method according to claim 17 as described above. Miller further taught wherein pointing an execution address to the secondary location further comprising inverting an address bit of the execution address [col. 6 lines 2-10 and col. 7 lines 4-7]. Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location.

10. As to claim 19, Miller taught the method according to claim 17 as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location [col. 6 line 33 through col. 7 line 7]. Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match.

11. As to claim 25, Miller taught the article according to claim 24 as described above. Miller also teaches claimed the method, therefore he also taught the claimed article comprising a medium for storing such instructions.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman et al, U.S. Patent 6,665,813 in view of Miller.

14. As to claim 6, Forsman taught a method comprising:

a. processor (processor 202 and processor 204) [figure 2];

b. a flash memory comprising a primary location (recovery code copy A) and a secondary location (recovery code copy B) [figures 3,4,5, col. 1 lines 49-52, and col. 5 line 44 through col. 6 line 59]; and

c. a boot block executed from the primary location, wherein the boot block further:

i. receives a second boot block (copy new recovery code - 502) into the secondary location (into recovery code copy B - 502) [figure 5 and corresponding text];11

ii. copies the second boot block (copy recovery code copy B into recovery code A - 408) to the primary location [figure 4];

iii. points the execution address (execute recover code copy A - step 416) to the primary location [figure 4].

Forsman does not expressly disclose wherein the boot block points an execution address to the secondary location. Forsman loads a new recovery copy into recovery code Copy B. However in Forsman, it is assumed that there are no problems when recovery code B is copied into recovery code A (set 408 of figure 4).

Miller teaches a boot block that points an execution address to a secondary location (CPU will boot from the secondary location, therefore an execution address must point to the secondary location) [col. 6 lines 4-10]. Miller teaches a system similar to that of Forsman. Miller is slightly different in that the boot blocks are copied in a slightly different manner. Miller points the execution address to the secondary location to ensure that if at a subsequent point the primary location becomes corrupted the system will still be able to boot using the secondary location. Miller points the execution address after a boot block is copied and validated.

It would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Forsman and Miller before him, to modify Forsman by pointing the execution address to the secondary location as taught by Miller immediately after copying the new recovery code into the secondary location at step 502.

One of ordinary skill in the art would have been motivated to make this modification in order to ensure that if at a subsequent point the primary location (copy A) becomes corrupted during the copying of B into A the system will still be able to boot using the secondary location (such as a problem with copying copy B into copy A at step 408).

15. As to claim 7, Forsman together with Miller taught the system according to claim 6, as described above. Miller further teaches an address conversion mechanism (boot in progress flag) for moving the execution address (flag determines where execution will begin) [col. 6 lines 2-10 and col. 7 lines 4-7].

16. As to claim 8, Forsman together with Miller taught the system according to claim 6, as described above. Forsman further teaches a non-volatile storage (firmware flash structure) for storing the second boot block (copy B) [figure 3].

17. As to claim 10, Miller taught the system according to claim 6 as described above. Miller teaches maintaining the state of an address bit ("sticky bit") following a power cycle (power failure, power up or a reset) [col. 5 line 65 through col. 6 line 10]. Specifically, Miller discloses using a flag that holds the state of an execution address bit. The flag is set in a latch or a flip-flop and is maintained during a power failure, power up or a reset.

Miller does not expressly disclose using a backup battery for maintaining the state of the address bit. Specifically, Miller is silent as to the power source used to maintain the state of the address bit. Miller suggests using a latch or flip-flop. In order for the state of the latches and flip-flops to be maintained power must be supplied to them. Thus, it is necessary in Miller that another power supply must supply power the latch or flip-flop. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a backup battery to supply power to the latch or flip-flop maintaining the state of the address bit. One of ordinary skill in the art would be motivated to use a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

18. As to claim 11, Miller taught the system according to claim 10 as described above. Miller further teaches that jumper may be used for adjusting the address bit [col. 7 line 63 through col. 8 line 34]. Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

Miller does not expressly disclose that the jumper is used when the backup battery fails. It would have been obvious to one of ordinary skill in the art use the jumper to adjust the address bit if hardware exists and the backup battery fails. One of ordinary skill in the art would recognized from the teaching of Miller that the address bit would still be adjustable by use of the jumper. One of ordinary skill would have been motivated to use the jumper because it would enable the user to set the address for execution even if the backup battery fails.

19. As to claims 1, 12 and 26, Forsman together with Miller taught the claimed system. Therefore, together they also teach the claimed method of using the system and the claimed article comprising a medium storing instructions.

20. As to claim 2, Forsman together with Miller taught the method according to claim 1, as described above. Miller further taught wherein pointing an execution address to the secondary location further comprising inverting an address bit of the execution address [col. 6 lines 2-10 and col. 7 lines 4-7]. Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1".

21. As to claim 3, Forsman together with Miller taught the method according to claim 2, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address [col. 8 lines 20-34].

22. As to claim 4, Forsman together with Miller taught the method according to claim 1, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location [col. 6 line 33 through col. 7 line

7]. Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match. Specifically,

23. As to claim 5, Forsman together with Miller taught the method according to claim 1, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed [col. 6 lines 2-10 and col. 7 lines 4-7]. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

24. As to claim 13, Forsman together with Miller taught the method according to claim 12. Miller further taught wherein pointing an execution address to the secondary location further comprising inverting an address bit of the execution address [col. 6 lines 2-10 and col. 7 lines 4-7]. Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location.

25. As to claim 14, Forsman together with Miller taught the method according to claim 13, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address [col. 8 lines 20-34].

26. As to claim 15, Forsman together with Miller taught the method according to claim 13, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location [col. 6 line 33 through col. 7 line 7]. Specifically, Miller discloses that the copying of boot block is complete when a comparison

between the primary location (first region) and the secondary location (second region) produces a match.

27. As to claim 16, Forsman together with Miller taught the method according to claim 13, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed [col. 6 lines 2-10 and col. 7 lines 4-7]. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

28. As to claims 27 and 28, Forsman together with Miller taught the method according to claim 26, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed [col. 6 lines 2-10, col. 7 lines 4-7 and col. 7 lines 22-62]. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0". Miller discloses that if the flag is set to "1" the execution address is pointed to the secondary location and to the primary location if it is set to "0". The flag corresponds to an address, specifically address bit A16, which will be modified accordingly.

29. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265.

30. As to claim 22, Miller taught the system according to claim 20 as described above. Miller teaches maintaining the state of an address bit ("sticky bit") following a power cycle (power

failure, power up or a reset) [col. 5 line 65 through col. 6 line 10]. Specifically, Miller discloses using a flag that holds the state of an execution address bit. The flag is set in a latch or a flip-flop and is maintained during a power failure, power up or a reset.

Miller does not expressly disclose using a backup battery for maintaining the state of the address bit. Specifically, Miller is silent as to the power source used to maintain the state of the address bit. Miller suggests using a latch or flip-flop. In order for the state of the latches and flip-flops to be maintained power must be supplied to them. Thus, it is necessary in Miller that another power supply must supply power the latch or flip-flop. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a backup battery to supply power to the latch or flip-flop m7aintaining the state of the address bit. One of ordinary skill in the art would be motivated to use a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

31. As to claim 23, Miller taught the system according to claim 22 as described above. Miller further teaches that jumper may be used for adjusting the address bit [col. 7 line 63 through col. 8 line 34]. Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

Miller does not expressly disclose that the jumper is used when the backup battery fails. It would have been obvious to one of ordinary skill in the art use the jumper to adjust the address bit if hardware exists and the backup battery fails. One of ordinary skill in the art would recognized from the teaching of Miller that the address bit would still be adjustable by use of the jumper. One of ordinary skill would have been motivated to use the jumper because it would enable the user to set the address for execution even if the backup battery fails.

32. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman and Miller and in further view of Hill et al., U.S. Patent 5,987,605.

33. As to claim 9, Forsman together with Miller taught the system according to claim 6, as described above. Forsman together with Miller does not express disclose a network interface card connecting a system to a network and for downloading the second boot block system.

However, Forsman teaches using a PCI bridge from which modems and network adapters may be used to connect the data processing system with multiple network computers. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forsman together with Miller by substituting a network interface card to connect to the network computers. Forsman would suggest one of ordinary skill in the art that substituting a network interface card would provide the same functions as network adapter.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,622,246 to Biondi. This patent teaches a system and method for erasing firmware.

U.S. Pat. No. 6,275,931 to Narayanaswamy et al. This patent teaches system and method for upgrading boot code.

U.S. Pat. No. 6,205,548 to Hasbun. This patent teaches a system and method for updating nonvolatile memory.

U.S. Pat. No. 5,987,605 to Hill et al. This patent teaches system and method for upgrading boot code using RAM and Flash memory.

U.S. Pat. No. 5,964,873 to Choi et al. This patent teaches system and method for upgrading firmware.

U.S. Pat. No. 5,701,492 to Wadsworth. This patent teaches a system and method for updating an eprom.

U.S. Pat. No. 5,568,641 to Nelson et al. This patent teaches system and method for upgrading flash memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
July 6, 2004

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